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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2112	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/980,098	ITAMI, SHINJI	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5,6,8 and 10-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5,6,8 and 10-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 8th of September 2005. Claims 5, 6, and 8 have been amended; no claim has been canceled; and claims 11-13 have been newly added since the RCE Non-Final Office Action was mailed on 8th of June 2005. Currently, claims 1, 3, 5, 6, 8, and 10-13 are pending in this Application.

Claim Objections

2. The claim 12 recites the subject matter "the trigger" in line 1. However, it has not been specifically clarified in the claim 12 and its intervening claims. Therefore, the Examiner presumes that the term "the trigger" could be considered as --the trigger signal-- in light of the prior claim 1 since it is not defined in the claims.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 5, 6 and 8 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

In fact, the claims 5, 6 and 8 recite the limitation "when a waveform is deformed by the trigger signal during the data transmission/reception, the memory start address is not incremented" in lines 21-22 of the claim 5, in lines 16-17 of the claim 6, and in lines 19-20 of the claim 8, respectively. However, the claimed limitation was not described in the specification in such a way as to reasonably convey to one

skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

5. Claim 12 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In fact, the trigger signal is not a toggling signal, but a falling edge triggered signal (See Figs. 5 and 8 in the Application). Therefore, the claimed subject matter "the trigger signal is toggled only in response to switching state of the cycle signal" is a new matter.

Furthermore, the Claim 12 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In fact, the trigger signal is not a toggling signal, which is evidently shown in Figs. 3, 6, 10, and 13 of the Application, and thus the Examiner doubts how the trigger signal could be toggled in response to switching state of the cycle signal (viz., PHASE signal).

Claim Rejections - 35 USC § 102

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. Claims 1, 3, 5, 6, 8, 10, 11, and 13 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant Admitted Prior Art [hereinafter AAPA].

Referring to claim 1, AAPA discloses a data transmission system (Fig. 16), comprising:

- a primary board (i.e., primary board 100 of Fig. 16);
- secondary boards (i.e., secondary boards A-C 200a-c in Fig. 16); and

- a data transmission path (i.e., data transmission bus 300 of Fig. 16) carrying out data transmission/reception (See page 1, lines 16-20) between said primary board (i.e., said primary board on the transmission transmitter side) and said secondary boards (i.e., said secondary boards on the transmission receiver side),
    - said data transmission path (i.e., said data transmission bus) employs a same signal line (A15:2/D15:0 206 of Figs. 17 and 19) as an address bus (i.e., Address 15:2) and a data bus (i.e., Data 15:0) mutually (See timing diagram for A15:2/D15:0 206 of Fig. 19 and page 2, lines 11-15), wherein
        - when said data access (i.e., Reading Process in Fig. 20) is executed from said primary board to said secondary boards (See Figs. 20 and 21), informing a start address (i.e., Step S211- A15:2/D15:0 START ADDRESS OUTPUT in Fig. 20) required for data access (See page 3, line 24 through page 4, line 4), and wherein
            - an address (i.e., a generated address based on Start Address A15:2 with signal A1:0 in Fig. 20) used in said data access (i.e., accessing DATA 1-4 in Fig. 19) in said secondary boards (i.e., said DATA 1-4 are in said secondary boards being addressed by said generated address; See page 4, lines 8-21) is generated based on said start address (i.e., said A15:2/D 15:0 START ADDRESS OUTPUT), a predetermined trigger signal (i.e., trigger signal TRG201 in Figs. 17 and 19) and a cycle signal (i.e., signal A1:0 (205) in Figs. 19 and 20) indicating switching of data (See page 5, lines 6-18), said cycle signal is combined with said trigger signal (i.e., said secondary board interprets said signal A1:0 and said trigger signal TRG as combined for outputting said DATA 1-4; See page 4, line 22 through page 5, line 18).

Referring to claim 3, AAPA teaches

- when said address (i.e., a generated address based on Start Address A15:2 with signal A1:0 in Fig. 20) is generated based on said trigger signal (i.e., trigger signal TRG201 in Figs. 17 and 19; See page 4, line 22 through page 5, line 5), said address is generated sequentially by incrementing said start address (i.e., said Start Address being incremented with A1:0 205 in sequence of 0h, 1h, 2h and 3h in Fig. 19) in response to a timing of said trigger signal (See trigger signal TRG201 and signal A1:0 (205) in Figs. 17 and 19, and page 5, lines 6-18).

Referring to claim 5, AAPA discloses a data transmission system (Fig. 16) comprising:

- a primary board (i.e., primary board 100 of Fig. 16);
- secondary boards (i.e., secondary boards A-C 200a-c in Fig. 16); and
- a data transmission path (i.e., data transmission bus 300 of Fig. 16) for carrying out data transmission/reception (See page 1, lines 16-20) between said primary board (i.e., said primary board on the transmission transmitter side) and said secondary boards (i.e., said secondary boards on the transmission receiver side), where
    - said data transmission path (i.e., said data transmission bus) employs a same signal line (A15:2/D15:0 206 of Figs. 17 and 19) as an address bus (i.e., Address 15:2) and a data bus (i.e., Data 15:0) mutually (See timing diagram for A15:2/D15:0 206 of Fig. 19 and page 2, lines 11-15), wherein:
        - when said data access (i.e., Reading Process in Fig. 20) is executed from said primary board to said secondary boards (See Figs. 20 and 21),

- informing a memory start address (i.e., Step S211- A15:2/D 15:0 START ADDRESS OUTPUT in Fig. 20) of said secondary boards required for data access (See page 3, line 24 through page 4, line 4),
- judging in said secondary boards is performing whether or not said memory start address is directed to own station (See page 2, line 25 through page 3, line 3; i.e., Separator 207 in Secondary Board 200 in Fig. 17 is performing the step S201 in Fig. 18), and then
- executing said data transmission via said data transmission path (i.e., data transmission bus) by accessing a memory (i.e., Memory 208 of Fig. 17) in own station (i.e., target Secondary Board 200 of Fig. 17) based on said memory start address when said memory start address is directed to own station (See page 3, lines 4-13 and Fig. 18), and

o an address (i.e., a generated address based on Start Address A15:2 with signal A1:0 in Fig. 20) is generated, to which said data transmission is subsequently executed (i.e., steps of S214-S220 in Fig. 20), in said secondary boards (i.e., address is constructed in said secondary boards by synthesizing the address A15:2/D15:0 assigned from said primary board; See page 4, line 24 through page 5, line 2) by

- incrementing said memory start address (i.e., said Start Address being incremented with A1:0 205 in sequence of 0h, 1h, 2h and 3h in Fig. 19) after said data transmission based on said memory start address is ended (i.e., steps of S211 and S212 in Fig. 20), and then
- executing said data transmission via said data transmission path by accessing said memory of own station (i.e., target Secondary Board) based on said generated address (See timing diagram in Fig. 19 and page 5, lines 6-18),

- wherein a cycle signal (i.e., signal A1:0 in Fig. 20) indicating switching of data (See page 5, lines 6-18) is used in combination with a trigger signal (i.e., said secondary board interprets said signal A1:0 and trigger signal TRG201 in Figs. 17 and 19 as combined for outputting said DATA 1-4; See page 4, line 22 through page 5, line 18),
- wherein when a waveform is deformed by said trigger signal during said data transmission/reception, said memory start address is not incremented (See Fig. 21, in fact, an address generation at Step S233 is not repeated (i.e., going to End of Reading Process at Step S232) for address increment when a waveform of FRAME is not L (i.e., Low) caused by signal deformation to H (i.e., High) in the middle of data accessing process by trigger signal TRG, e.g., a noisy trigger signal, inherently anticipates that when a waveform is deformed by said trigger signal during said data transmission/reception, said memory start address is not incremented. In other words, a synthesized address construction, which is based on Start Address A15:2/D15:0 (206) with signal A1:0 (205), is not repeated, viz., no address increment, when a waveform of FRAME 202 is deformed to H (i.e., High) in the middle of data accessing process by a noise from trigger signal TRG201, for example, in Fig. 19), and
- wherein said secondary board does not shift to a next process until said cycle signal (i.e., signal A0 of said signal A1:0) has been toggled (See page 4, lines 8-21; i.e., the secondary board does not proceed to the next process S234 Memory Read in Fig. 21 until the bus direction has been

changed from input to output, and the cycle has been switched from the address cycle to the data reading cycle), and leading and trailing edges of said trigger signal are detected in combination with detecting said toggle states of said cycle signal (See page 4, line 15 through page 5, line 3).

Referring to claim 6. AAPA discloses a method of transmitting data by a data transmission system (See page 1, line 14 through page 2, line 2 and Fig. 16) comprising a primary board (i.e., primary board 100 of Fig. 16), secondary boards (i.e., secondary boards A-C 200a-c in Fig. 16), and a data transmission path (i.e., data transmission bus 300 of Fig. 16) for carrying out data read (See page 1, lines 16-20 and page 3, lines 14+) between said primary board (i.e., said primary board on the transmission transmitter side) and said secondary boards (i.e., said secondary boards on the transmission receiver side), wherein said data transmission path (i.e., said data transmission bus) employs a same signal line (i.e., A15:2/D15:0 206 of Figs. 17 and 19) as an address bus (i.e., Address 15:2) and a data bus (i.e., Data 15:0) mutually (See timing diagram for A15:2/D15:0 206 of Fig. 19 and page 2, lines 11-15), said method comprising:

- informing a trigger signal (i.e., trigger signal TRG201 in Figs. 17 and 19) combined with a cycle signal (i.e., signal A1:0 in Fig. 19; in fact, said secondary board interprets said signal A1:0 and said trigger signal TRG as combined for outputting said DATA 1-4; See page 3, line 24 through page 4, line 4) indicating a timing of data access (See page 4, line 22 through page 5, line 20), and a start address (i.e., Step S211- A15:2/D15:0 START ADDRESS OUTPUT in Fig. 20) required for data read (i.e., data reading in Figs. 20 and 21) via said data transmission path (i.e., data transmission bus);
- switching said data transmission path to which said start address is informed as a data bus (See timing diagram A15:2/D15:0 (206) in Fig. 19);

- accessing a memory (i.e., Memory 208 of Fig. 17) based on said start address (i.e., ADDRESS of A15:2/D15:0 (206) and A1:0 (205) in Fig. 19 and Steps of S211 and S214 in Fig. 20) and sending out a read result onto said data transmission path (See page 5, lines 4-5); and
- incrementing said start address (i.e., said Start Address being incremented with A1:0 (205) in sequence of 0h, 1h, 2h and 3h in Fig. 19), and then sending out a read result onto said data transmission path by accessing said memory based on said incremented address (See timing diagram in Fig. 19 and page 5, lines 8-20),
    - wherein said start address is not incremented when a waveform is deformed by said trigger signal during said data read (See Fig. 21, in fact, an address generation at Step S233 is not repeated (i.e., going to End of Reading Process at Step S232) for address increment when a waveform of FRAME is not L (i.e., Low) caused by signal deformation to H (i.e., High) in the middle of data accessing process by trigger signal TRG, e.g., a noisy trigger signal, inherently anticipates that said start address is not incremented when a waveform is deformed by said trigger signal during said data read. In other words, a synthesized address construction, which is based on Start Address A15:2/D15:0 (206) with signal A1:0 (205), is not repeated, viz., no address increment, when a waveform of FRAME 202 is deformed to H (i.e., High) in the middle of data accessing process by a noise from trigger signal TRG201, for example, in Fig. 19), and
    - wherein said secondary board does not shift to a next process until said cycle signal (i.e., signal A0 of said signal A1:0) has been toggled (See page 4, lines 8-21; i.e., the secondary board does not proceed to the next process S234 Memory Read in Fig. 21 until the bus direction has been changed from input to output, and the cycle has been switched from the address cycle to the data reading cycle), and leading and trailing edges of said

trigger signal are detected in combination with detecting said toggle states of said cycle signal (See page 4, line 15 through page 5, line 3).

Referring to claim 8, AAPA discloses a data transmission system (Fig. 16) comprising:

- a primary board (i.e., primary board 100 of Fig. 16);
- secondary boards (i.e., secondary boards A-C 200a-c in Fig. 16); and
- a data transmission path (i.e., data transmission bus 300 of Fig. 16) for carrying out data write (See page 1, lines 16-20 and page 5, lines 21+) between said primary board (i.e., said primary board on the transmission transmitter side) and said secondary boards (i.e., said secondary boards on the transmission receiver side), where said data transmission path (i.e., said data transmission bus) employs a same signal line (A15:2/D15:0 206 of Figs. 17 and 22) as an address bus (i.e., Address 15:2) and a data bus (i.e., Data 15:0) mutually (See timing diagram for A15:2/D15:0 206 of Fig. 22 and page 2, lines 11-15), wherein
    - said carrying out of said data write (i.e., --Writing Process-- on page 5) is executed by:
        - informing a trigger signal (i.e., trigger signal TRG201 in Figs. 17 and 22) combined with a cycle signal (i.e., signal A1:0 in Fig. 22; in fact, said secondary board interprets said signal A1:0 and said trigger signal TRG as combined for outputting said DATA 1-4; See page 6, lines 17-24) indicating a timing of data access (See page 6, line 25 through page 7, line 11) and a start address (i.e., Step S241- A15:2/D15:0 START ADDRESS OUTPUT in Fig. 23) required for data write (i.e., data writing in Figs. 23 and 24) via said data transmission path (i.e., said data transmission bus),
        - switching said data transmission path to which said start address is informed as a data bus (See timing diagram A15:2/D15:0 (206) in Fig. 22), and then sending

out a predetermined data (i.e., Data 1 in step S242 in Fig. 23) to be written to a memory (i.e., Memory 208 of Fig. 17);

- accessing said memory (i.e., Memory) based on said start address (i.e., ADDRESS of A15:2/D15:0 (206) and A1:0 (205) in Fig. 22 and Steps of S241 and S242 in Fig. 23), and then writing said predetermined data to be written into said memory (See page 6, lines 6-16),
- incrementing said start address (i.e., said Start Address being incremented with A1:0 205 in sequence of 0h, 1h, 2h and 3h in Fig. 22), and then writing sequentially said predetermined data (i.e., Data 2-4 in steps S244, S246 and S248 in Fig. 23), that are sent out via said data transmission path (i.e., Data Bus), into said memory by accessing said memory based on said incremented address (See timing diagram in Fig. 22 and page 6, line 17 through page 7, line 6),
- detecting leading and trailing edges of said trigger signal in combination with detecting toggle states of said cycle signal (i.e., detecting TRG with detecting toggle states of Addressing cycle phase and Data cycle phase in Fig. 22; See page 6, line 17 through page 7, line 1),
- not incrementing said start address when a waveform is deformed by said trigger signal during said data write (See Fig. 24, in fact, an address generation at Step S262 is not repeated (i.e., going to End of Writing Process at Step S261) for address increment when a waveform of FRAME is not L (i.e., Low) caused by signal deformation to H (i.e., High) in the middle of data writing process by trigger signal TRG, e.g., a noisy trigger signal, inherently anticipates that said address is not incremented when a waveform is deformed by said trigger signal. In other words, a synthesized address construction, which is based on Start

Address A15:2/D15:0 (206) with signal A1:0 (205), is not repeated, viz., no address increment, when a waveform of FRAME 202 is deformed to H (i.e., High) in the middle of data writing process by a noise from trigger signal TRG201, for example, in Fig. 22), and

- not shifting said secondary board to a next process until said cycle signal has been toggled (See page 6, lines 15-24; i.e., the secondary board does not proceed to the next process S264 Memory Write in Fig. 24 until the cycle has been switched from the address cycle to the data reading cycle).

Referring to claim 10, AAPA discloses a method for carrying out data write (See page 1, lines 16-20 and page 5, lines 21+) between a primary board (i.e., primary board 100 of Fig. 16 on the transmission transmitter side) and secondary boards (i.e., secondary boards A-C 200a-c in Fig. 16 on the transmission receiver side) by using a data transmission path (i.e., data transmission bus 300 of Fig. 16), which employs a same signal line (A15:2/D15:0 206 of Figs. 17 and 22) as an address bus (i.e., Address 15:2) and a data bus (i.e., Data 15:0) mutually (See timing diagram for A15:2/D15:0 206 of Fig. 22 and page 2, lines 11-15), comprising:

- informing a trigger signal (i.e., trigger signal TRG201 in Figs. 17 and 22) combined with a cycle signal (i.e., signal A1:0 in Fig. 22; in fact, said secondary board interprets said signal A1:0 and said trigger signal TRG as combined for outputting said DATA 1-4; See page 6, lines 17-24) indicating a timing of data access (See page 6, line 25 through page 7, line 11) and a start address (i.e., Step S241-A15:2/D15:0 START ADDRESS OUTPUT in Fig. 23) required for data write (i.e., data writing in Figs. 23 and 24) via said data transmission path (i.e., data transmission bus);

- switching said data transmission path to which said start address is informed as a data bus (See timing diagram A15:2/D15:0 (206) in Fig. 22), and then sending out a predetermined data (i.e., Data 1 in step S242 in Fig. 23) to be written to a memory (i.e., Memory 208 of Fig. 17);
- accessing said memory (i.e., Memory) based on said start address (i.e., ADDRESS of A15:2/D15:0 (206) and A1:0 (205) in Fig. 22 and Steps of S241 and S242 in Fig. 23), and then writing said predetermined data to be written into said memory (See page 6, lines 6-16);
- incrementing said start address (i.e., said Start Address being incremented with A1:0 (205) in sequence of 0h, 1h, 2h and 3h in Fig. 22), and then writing sequentially said predetermined data (i.e., Data 2-4 in steps S244, S246 and S248 in Fig. 23), that are sent out via said data transmission path (i.e., Data Bus), into said memory by accessing said memory based on said incremented address (See timing diagram in Fig. 22 and page 6, line 17 through page 7, line 6).

Referring to claim 11, AAPA teaches

- said cycle signal (i.e., signal A1:0 (205) in Figs. 19 and 20) only indicates said switching of said data (See page 5, lines 6-18; i.e., said signal A1:0 only indicates switching data cycle 0h, 1h, 2h, and 3h in Fig. 19, for example).

Referring to claim 13, AAPA teaches

- said secondary board (i.e., secondary boards A-C 200a-c in Fig. 16) generates (i.e., synthesizes) subsequent addresses used in data access based on said start address (See page 4, line 22 through page 5, line 5) and
    - wherein said subsequent addresses (i.e., continuous memory read addresses) are generated by said secondary board (i.e., being synthesized by said second board at step S233 in Fig. 21) by incrementing last address used (i.e., in fact that DATA1, DATA2,

DATA3, and DATA4 are addressed using Starting address ADDRESS on A15:2/D15:0 (206) and incremental data on A1:0 (205) after being synthesized by said second board in Fig. 19).

Response to Arguments

8. Applicant's arguments filed on 8th of September 2005 have been fully considered but they are not persuasive.

In response to the Applicant's argument with respect to claims 5, 6, and 8 rejection under 35 U.S.C. § 112, first paragraph in the Response pages 10-11, the Examiner believes that the Applicant misinterprets the claim rejection.

In fact, the Applicant argues that the original specification supports the claimed limitation "the address is not incremented during the time in which the waveform is deformed by the trigger signal" on pages 26, 27, 38, and 39. However, in contrary to the Applicant's arguments, the original specification is silent to disclose that the waveform is deformed by the trigger signal.

Moreover, it is noted that the features upon which applicant relies (i.e., the waveform is deformed by the noise) are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Thus, the Applicant's argument on this point is not persuasive.

In response to the Applicant's argument with respect to "In order to somehow meet the unique features of claim 1, the Examiner alleges that "informing a start address required for access" is disclosed in step 211 of the APA i.e., Start Address A15:2, and that ... Applicant respectfully disagrees. As disclosed by the APA, the signal A1:0 simply indicates the lower two bits of the data transmission bus (page 2 of the specification). That is, the signal A1:0 is used for outputting the lower bits of the address. That is, the signal A1:0 is not indicating the switching of data. ... Accordingly, the lower addresses signal

lines are not necessary and the continuous transmission can be accomplished via fewer signal lines by incrementing the previous address used. ..." in the Response page 12, line 4 through page 13, line 11, the Examiner respectfully disagrees.

In contrary to the Applicant's allegation, AAPA suggests a signal A1:0 (205), i.e., cycle signal, indicating switching of data DATA1, DATA2, DATA3, and DATA4 in Fig. 19 (See Application, page 5, lines 6-18). In other words, when said signal A1:0 is 0h, then it indicates switching to DATA1, when said signal A1:0 is 1h, then it indicates switching to DATA2, when said signal A1:0 is 2h, then it indicates switching to DATA3, and when said signal A1:0 is 3h, then it indicates switching to DATA4.

Furthermore, in contrary to the Applicant's assertion, the lower addresses signal lines are absolutely necessary for the claimed subject matter "start address" in the claimed invention and the continuous transmission cannot be accomplished via fewer signal lines because the lower addresses signal lines are still necessary in the claimed invention. This is clearly shown in the Figs. 2 and 10, such that A**15:0**/D**15:0** (25).

Thus, the Applicant's argument on this point is not persuasive.

In response to the Applicant's argument with respect to "... The Examiner alleges that since the address is not incremented when the FRAME signal is high, it inherently anticipates that the address is not incremented when the waveform is deformed by the trigger signal (*see* page 8 of the Office Action). In the present case, in the APA, the address is changed when the trigger signal is raised, e.g. *see* T43, T44, and so on, page 5 of the specification. Accordingly, the APA does not teach or suggest not incrementing the memory start address during the waveform deformation by the trigger signal. ... In short, the APA fails to teach or suggest when a waveform is deformed by the trigger signal during the data transmission/reception, not incrementing the memory start address." in the Response page 13, line 12 through page 14, line 5, the Examiner respectfully disagrees.

In fact, AAPA discloses that the secondary board does not effectively increment the memory address (i.e., not synthesizing memory address) during the waveform FRAME deformation (e.g., being set to H by triggering noise) because the secondary board quits the read/write operation during the waveform FRAME deformation even though the address lines inform the memory access addresses to the secondary board (See Fig. 22 as an example).

Thus, the Applicant's argument on this point is not persuasive.

In response to the Applicant's argument with respect to "Furthermore, claim 5 recites: "wherein the secondary board does not shift to a next process until the cycle signal has been toggled, and leading and trailing edges of the trigger signal are detected in combination with detecting the toggle states of the cycle signal." The Examiner alleges that this unique feature of claim 5 is disclosed by the reading process disclosed in the APA. If, however, as alleged by the Examiner, the address signal A1:0 is equivalent to the cycle signal, then the APA clearly does not teach or suggest toggling this address signal in combination with the trigger signal *see e.g.,* Figs. 19 and 21. Moreover, in the APA, there is no cycle signal. For at least these additional reasons, it is respectfully submitted that claim 5 is patentable over the APA." in the Response page 14, lines 6-14, the Examiner respectfully disagrees.

In contrary to the Applicant's statement, AAPA clearly suggests toggling the address signal A1:0, such that the signal A0 of said A1:0 is changing in accordance with the sequence of 0,1,0,1,..., i.e., toggling, in combination with the trigger signal TRG in Figs. 19 and 21 (See AAPA, page 4, line 15 through page 5, line 3).

Thus, the Applicant's argument on this point is not persuasive.

9. Applicant's arguments with respect to claims 6 and 11-13 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher E. Lee
Examiner
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